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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
09/498,525	02/04/2000	Hammam Elabd	73234	8921	
5	7590 04/22/2003				
	dison & Sutro LLP	EXAMINER			
Ninth Floor Ea		VO, LILIAN			
Washington, DC 20005-3918			ART UNIT	PAPER NUMBER	
			2127	7	
			DATE MAILED: 04/22/2003	DATE MAILED: 04/22/2003	

Please find below and/or attached an Office communication concerning this application or proceeding.

-6		,	Application No.	Applicant(s)	
Offic Action Sum			09/498,525	ELABD, HAMMAM	
		Action Summary	Examiner	Art Unit	_
}			Lilian Vo	2127	
Peri d fo	The MAIL	LING DATE of this communication ap			
A SH THE - Exte - If the - If the - If NC - Failu - Any	MAILING Densions of time in SIX (6) MONTH e period for reply ure to reply within reply received by	O STATUTORY PERIOD FOR REPL DATE OF THIS COMMUNICATION. hay be available under the provisions of 37 CFR 1. HS from the mailing date of this communication. by specified above, the maximum statutory period on the set or extended period for reply will, by statut by the Office later than three months after the mailing adjustment. See 37 CFR 1.704(b).	136(a). In no event, however, may a reply be timely within the statutory minimum of thirty (30) daywill apply and will expire SIX (6) MONTHS from e. cause the application to become ARANDONE.	nely filed  s will be considered timely. the mailing date of this communication  1. (35.1) S.C. 8.133	on.
1)⊠	Responsi	ive to communication(s) filed on <u>04</u>	<u>February 2000</u> .		
2a)□	This action	on is <b>FINAL</b> . 2b)⊠ TI	his action is non-final.		
3)□ Disp siti	Since this closed in ion of Clair	s application is in condition for allow accordance with the practice under ms	ance except for formal matters, professional Exparte Quayle, 1935 C.D. 11, 4	osecution as to the merits 53 O.G. 213.	is
4)⊠	Claim(s)	1-32 is/are pending in the application	n.		
	4a) Of the	above claim(s) is/are withdra	wn from consideration.		
5)	Claim(s) _	is/are allowed.			
6)[	Claim(s) _	is/are rejected.			
7)	Claim(s) _	is/are objected to.			
8)⊠	Claim(s) 1	-32 are subject to restriction and/or	election requirement.		
Applicati	on Papers		·		
9) 🔲 -	The specific	cation is objected to by the Examine	er.		
10) 🔲 🗆	The drawing	g(s) filed on is/are: a)□ acce	pted or b)⊡ objected to by the Exan	niner.	
	Applicant i	may not request that any objection to th	e drawing(s) be held in abeyance. Se	e 37 CFR 1.85(a).	
11) 🔲 🛚	The propos	ed drawing correction filed on	_ is: a) ☐ approved b) ☐ disapprov	ved by the Examiner.	
	If approve	d, corrected drawings are required in re	ply to this Office action.		
12) 🔲 🛭	The oath or	declaration is objected to by the Ex	aminer.		
Pri rity u	nder 35 U.	S.C. §§ 119 and 120			
13)	Acknowled	gment is made of a claim for foreigr	n priority under 35 U.S.C. § 119(a)	-(d) or (f).	
a)[	□All b)□	Some * c)  None of:			
	1. Certi	ified copies of the priority document	s have been received.		
	2. Certi	ified copies of the priority document	s have been received in Application	n No	
	·a	es of the certified copies of the prior application from the International Bu ched detailed Office action for a list	reau (PCT Rule 17.2(a)).	J	
14) 🗌 A	cknowledgr	ment is made of a claim for domesti	c priority under 35 U.S.C. § 119(e)	(to a provisional applicati	on).
_a)	☐ The tra	inslation of the foreign language proment is made of a claim for domesti	ovisional application has been rece	ived.	ŕ
Attachment	(s)				
2) Notice	of Draftspers	es Cited (PTO-892) son's Patent Drawing Review (PTO-948) ure Statement(s) (PTO-1449) Paper No(s)	5) Notice of Informal Pa	PTO-413) Paper No(s) atent Application (PTO-152)	
S. Patent and Tra TO-326 (Rev		Office Ac	tion Summary	Part of Paper No.	3

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## **DETAILED ACTION**

## Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

**Group I,** claims 1 - 14, which drawn to a system for providing parallel processing of data to a plurality of DSPs with program/data memory and ping-pong memory interface, and how the communication data is transmitted, classified in class 709, subclass 250.

**Group II,** claims 15 – 30, which drawn to a DSP load management system, which also include a decoder for decoding instructions such as load and algorithm switching instructions to provide optimal processing, classified in class 709, subclass 212.

**Group III,** claims 21 – 30, which drawn to a method of providing parallel processing of data to a plurality of DSPs which write the communication data to a selected register from a plurality of registers, wherein the register is selected based on the current load status and different algorithms loaded, classified in class 709, subclass 200.

**Group IV,** claims 31-32, which drawn to a method of optimizing the processing capabilities of a plurality of digital signal processors on an SOC devices having a DSP load management system with inter-transaction, intra-transaction, and hardware mapping optimizations, classified in class 709, subclass 223.

2. The inventions are distinct, each from the other because of the following reasons: Inventions I - IV are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be

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separately usable. In the instant case, invention I has separate utility such as in a system lacking a decoder for decoding instructions such as load and algorithm switching instructions to provide optimal processing, the writing of the communication data to a selected register from a plurality of registers, wherein the register is selected based on the current load status and different algorithms loaded, and a method of optimizing the processing capabilities of a plurality of digital signal processors on an SOC devices having a DSP load management system with intertransaction, intra-transaction, and hardware mapping optimizations. Invention II has separate utility such as in a system lacking the writing of the communication data to a selected register from a plurality of registers, wherein the register is selected based on the current load status and different algorithms loaded, and a method of optimizing the processing capabilities of a plurality of digital signal processors on an SOC devices having a DSP load management system with inter-transaction, intra-transaction, and hardware mapping optimizations. Invention III has separate utility such as in a system lacking a method of optimizing the processing capabilities of a plurality of digital signal processors on an SOC devices having a DSP load management system with inter-transaction, intra-transaction, and hardware mapping optimizations. See MPEP § 806.05(d).

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

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4. Because these inventions are distinct for the reasons given above and the search required

for one group is not required for another group, restriction for examination purposes as indicated

is proper.

5. A telephone call was made to Chang Kim on 4/15/2003 to request an oral election to the

above restriction requirement, but did not result in an election being made.

6. Applicant is advised that the reply to this requirement to be completed must include an

election of the invention to be examined even though the requirement be traversed (37 CFR

1.143).

7. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Lilian Vo whose telephone number is 703-305-7864.

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the receptionist whose telephone number is 703-305-3900.

Lilian Vo

Examiner

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lv April 17, 2003

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